UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,157	12/02/2003	Richard Thomas Plunkett	PEA08US	6698

24011 7590 04/04/2008
SILVERBROOK RESEARCH PTY LTD
393 DARLING STREET
BALMAIN, 2041
AUSTRALIA

EXAMINER	
CHRZANOWSKI, MATTHEW R	
ART UNIT	PAPER NUMBER
2186	
MAIL DATE	DELIVERY MODE
04/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,157	PLUNKETT, RICHARD THOMAS	
	Examiner	Art Unit	
	MATTHEW R. CHRZANOWSKI	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

2. Claim 6 objected to because of the following informalities: misspelled word, “acess”. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 1-18** rejected under 35 U.S.C. 112, first and second paragraphs, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant recites support for the amendments (specifically those found in the independent claims 1, 6, and 10), "can be found at paragraphs [2209]-[2239] of the present specification" *(Remarks/Arguments: page 6)*. It is noted that the specification submitted to the office does not contain paragraph numbers but instead page and line numbers, therefore it is assumed Applicant is referring to the publication of this application, US 20050177633. These paragraphs show support for "busses" and data being sent on these busses, however, the claim language is not shown in the cited sections, and furthermore elsewhere in the specification. The claim language, "receive a plurality of access requests on a plurality of data busses, the first type of access request being received on a different data bus than the other types of access requests" is found to be new matter. Dependent **claims 2-5, 7-8, and 11-18** inherit these defects.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 1-5** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")** in view of **Non-Patent Literature ("Southbridge – a whatis definition," Jason Rush, hereinafter "NPL1")** and **Non-Patent Literature ("RIOT-The Scheduling Problem," hereinafter "NPL2")**.

Consider **claim 1**, Stacovsky discloses a method for arbitrating between a plurality of access requests issued in relation to a resource by a plurality of requesters *(FIG. 9A-B, 14)*, wherein each request can be one of at least two types, a first of the types having a higher latency associated with its performance than at least some of the other types *(it can but not necessarily does; in a system with different processors and memories it is inherit that that there will be access requests of varying latencies, such as different distances between specific processors and memories, and fabrication/manufacturing defects)*, the method including the steps of:

(a) receiving a plurality of the access requests *(commands 1, 2: FIG. 14)* on a plurality of data busses *(system buses 106: FIG. 1A)*, a type of access request being received on a different data bus than the other types of access requests *(each from different systems 102: FIG. 1A)*;

(b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue; use of FIFO memory: column 18, line 19-20; FIG. 18)*; and

(c) in the event an access request as arbitrated via the lookahead pointer, initiating performance of the access request earlier than the position in the list suggests it would be performed should it be started when the current pointer reached the timeslot *(command 3 is executed before command 2, but after 1: FIG. 14)*.

Stacovsky discloses the use of a FIFO and executing requests out-of-order if prioritized as discussed above, and asserts it is inherit to a FIFO to (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list. However, if the applicant references FIFO that does not maintains these pointers, Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention a First-in-first-out or ordered buffer allows (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue)*, because a use of these buffers are a well-known way of indicating order of requests to indicate

priority based on order in which the entries were received. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Stacovsky discloses multiple system buses with access requests from those busses received by the universal device controller to access memories/shared resources *(FIG. 1A)*, but may not specifically disclose the first type, with higher latency associated with its performance, of access request being received on a different data bus than the other types of access requests. Stacovsky orders based on timeslot and prioritizes certain requests, however, Stacovsky may not specifically disclose prioritizing based on if the request **is of the first type** (if first type, initiate performance earlier than normal position of FIFO).

NPL1 discloses a system with a plurality of buses and a first type, with higher latency associated with its performance, of access request being received on a different data bus than the other types of access requests *(computer chipset including southbridge and northbridge; USB and ISA has higher latencies and be a slower bus over newer buses such as PCI and AGP buses: page 1)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have a first type, with higher latency associated with its performance, of access request being received on a different data bus than the other types of access requests (a chipset controlling multiple buses) in the system of Stacovsky, because NPL1 shows multiple buses

implemented in a system which would allow for multiple different connections to different peripheral devices. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Furthermore, NPL2 discloses a system which prioritizing higher latency requests earlier than normal ordered operation *(Longest Processing Time (LPT): page 1)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to prioritizing based on if the request is of the first type in the system of Stacovsky and NPL1, because NPL2 teaches the LPT is a heuristic used for finding the minimum makespan of a schedule and no one large job will "stick out" at the end of the schedule and dramatically lengthen the completion time of the last job *(page 1)*. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp *(LPT scheduling algorithm)*.

Consider **claims 2**, and as applied to **claim 1** above, Stacovsky in view of NPL1 and NPL2 disclose the method wherein step (c) includes the substep of performing the access request indicated by the lookahead pointer immediately after the access request indicated by the current pointer is performed *(Stacovsky: command 3 is executed before command 2, but immediately after command 1: FIG. 14)*.

Consider **claim 3**, and as applied to **claim 1** above, Stacovsky in view of NPL1 and NPL2 disclose the method wherein the first type of access request is a memory write request *(Stacovsky: column 9, lines 3-5)*.

Consider **claims 4**, and as applied to **claim 3** above, Stacovsky in view of NPL1 and NPL2 disclose the method wherein step (c) includes the substep of performing the access request indicated by the lookahead pointer immediately after the access request indicated by the current pointer is performed *(Stacovsky: command 3 is executed before command 2, but immediately after command 1: FIG. 14)*.

Consider **claim 5**, and as applied to **claim 1** above, Stacovsky in view of NPL1 and NPL2 disclose the method wherein the number of timeslots between the timeslot indicated by the lookahead pointer and the timeslot indicated by the current pointer takes into account a latency difference between performing an access request of the first type and at least one of the other access request types *(Stacovsky: the timeslots or entries "take into account" the latency difference because they arrive in order of receipt even though relative to time one of higher latency could have been sent before a lower latency time request but received by the arbiter afterwards; NPL2: Furthermore, takes into account priority and latency: page 1)*.

8. **Claim 10-16** rejected under 35 U.S.C. 103(a) as being unpatentable by **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")** in view of **Non-Patent Literature ("Southbridge – a whatis definition," Jason Rush, hereinafter "NPL1")**.

Consider **claim 10**, Stacovsky discloses a method of arbitrating between access requests from a plurality of requestors for access to a resource *(FIG. 9A-B, FIG. 14)*, wherein at least one of the requestors is defined as higher priority access to the resource *(column 8, lines 35-48)*, the method comprising the steps of:

(a) receiving a plurality of the access requests *(commands 1, 2: FIG. 14)* on a plurality of data busses *(system buses 106: FIG. 1A)*, a type of access request being received on a different data bus than the other types of access requests *(each from different systems 102: FIG. 1A)*;

(b) in the event an access request from the at least one of the requestors is received, initiating performance of the access request in preference to the requestor as specified by the timeslot list and regardless of whether or not the at least one of the requestors is in the timeslot list *(FIFO: FIG. 14)*.

Stacovsky discloses multiple system buses with access requests from those buses received by the universal device controller to access

memories/shared resources *(FIG. 1A)*, but may not specifically disclose the first type, with higher latency associated with its performance, of access request being received on a different data bus than the other types of access requests.

NPL1 discloses a system with a plurality of buses and a first type, with higher latency associated with its performance, of access request being received on a different data bus than the other types of access requests *(computer chipset including southbridge and northbridge; USB and ISA has higher latencies and be a slower bus over newer buses such as PCI and AGP buses: page 1)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have a first type, with higher latency associated with its performance, of access request being received on a different data bus than the other types of access requests (a chipset controlling multiple buses) in the system of Stacovsky, because NPL1 shows multiple buses implemented in a system which would allow for multiple different connections to different peripheral devices. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Consider **claim 11**, and as applied to **claim 10** above, Stacovsky in view of NPL1 discloses the method wherein the at least one requestor requires lower latency access to the resource than at least one of the other requestors from which access requests can be received *(in a system with different processors*

and memories it is inherit that that there will be access requests of varying latencies, such as different distances between specific processors and memories, and fabrication/manufacturing defects).

Consider **claim 12**, and as applied to **claim 10** above, Stacovsky in view of NPL1 discloses the method wherein the at least one requestor is a processor *(FIG. 9A-B, 14)*.

Consider **claim 13**, and as applied to **claim 10** above, Stacovsky in view of NPL1 discloses the method wherein the resource is a memory *(FIG. 9A-B, 14)*.

Consider **claim 14**, and as applied to **claim 10** above, Stacovsky in view of NPL1 discloses the method wherein step (b) includes the substep of performing the access request from the requestor immediately following completion of any current access request being reformed *(command 3 is executed before command 2, but immediately after command 1: FIG. 14)*.

Consider **claim 15**, and as applied to **claim 10** above, Stacovsky in view of NPL1 discloses the method wherein step (b) is performed such that a frequency of the at least one requestor being granted preferential performance of its access requests *(FIG. 14)* is limited within a time period *(In order to prevent what is referred to as livelock, a livelock counter register 156 contains information*

about the number of consecutive requests (or responses) with the higher priority which can bypass requests (or responses) with a lower priority. In this way, the lower priority request (or response) can not be starved for a substantial number of clock cycles: column 8, lines 35-48; and in the case there is only one requestor making the requests and therefore only being granted preferential performance, the livelock counter registers is of the one requestor).

Consider **claim 16**, and as applied to **claim 15** above, Stacovsky in view of NPL1 discloses the method wherein early performance of access requests from the at least one requestor is restricted to a maximum number of times within a predetermined number of timeslots *(In order to prevent what is referred to as livelock, a livelock counter register 156 contains information about the number of consecutive requests (or responses) with the higher priority which can bypass requests (or responses) with a lower priority. In this way, the lower priority request (or response) can not be starved for a substantial number of clock cycles.: column 8, lines 35-48; and in the case there is only one requestor making the requests and therefore only being granted preferential performance, the livelock counter registers is of the one requestor).*

9. **Claims 6-9** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")** in view of **Non-Patent Literature ("Southbridge – a whatis definition," Jason Rush, hereinafter**

"NPL1"), Non-Patent Literature ("RIOT-The Scheduling Problem," hereinafter "NPL2") and **Radke et al. (US Patent # 6741253 B2, hereinafter "Radke")**.

Consider **claim 6**, Stacovsky discloses an plurality of integrated circuit including: a plurality of operative units, each of which is capable of issuing a request for access to a memory accessible by the integrated circuit *(FIG. 1A, 9A-B, 14)*; and an timeslot arbitrator for arbitrating between requests issued by the operative units for access to the memory *(FIG. 14)*, wherein each request can be one of at least two types, a first of the types having a higher latency associated with its performance than at least some of the other types *(it can but not necessarily does; in a system with different processors and memories it is inherit that that there will be access requests of varying latencies, such as different distances between specific processors and memories, and fabrication/manufacturing defects)*, the timeslot arbitrator being configured to:

(a) receiving a plurality of the access requests *(commands 1, 2: FIG. 14)*;

(b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue; use of FIFO memory: column 18, line 19-20)*; and

(c) in the event an access request as arbitrated via the lookahead pointer, initiating performance of the access request earlier than the position in the list suggests it would be performed should it be started when the current pointer reached the timeslot *(command 3 is executed before command 2, but after 1: FIG. 14)*.

Stacovsky discloses the use of a FIFO and executing requests out-of-order if prioritized as discussed above, and asserts it is inherit to a FIFO to (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list. However, if the applicant references FIFO that does not maintains these pointers, Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention a First-in-first-out or ordered buffer allows (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue)*, because a use of these buffers are a well-known way of indicating order of requests to indicate priority based on order in which the entries were received. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Stacovsky discloses multiple system buses with access requests from those busses received by the universal device controller to access

memories/shared resources *(FIG. 1A)*, but may not specifically disclose the first type, with higher latency associated with its performance, of access request being received on a different data bus than the other types of access requests. Stacovsky orders based on timeslot and prioritizes certain requests, however, Stacovsky may not specifically disclose prioritizing based on if the request **is of the first type** (if first type, initiate performance earlier than normal position of FIFO).

NPL1 discloses a system with a plurality of buses and a first type, with higher latency associated with its performance, of access request being received on a different data bus than the other types of access requests *(computer chipset including southbridge and northbridge; USB and ISA has higher latencies and be a slower bus over newer buses such as PCI and AGP buses: page 1)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have a first type, with higher latency associated with its performance, of access request being received on a different data bus than the other types of access requests (a chipset controlling multiple buses) in the system of Stacovsky, because NPL1 shows multiple buses implemented in a system which would allow for multiple different connections to different peripheral devices. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Furthermore, NPL2 discloses a system which prioritizing higher latency requests earlier than normal ordered operation *(Longest Processing Time (LPT): page 1)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to prioritizing based on if the request is of the first type in the system of Stacovsky and NPL1, because NPL2 teaches the LPT is a heuristic used for finding the minimum makespan of a schedule and no one large job will "stick out" at the end of the schedule and dramatically lengthen the completion time of the last job *(page 1)*. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp *(LPT scheduling algorithm)*.

Furthermore, Radke discloses placing processors and memory on an embedded/integrated circuit *(column 1, lines 14-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made integrate the entire processors, memory and arbitrator in the system of Stacovsky in view of NPL1 and NPL2, because it is a design choice which increases throughput of processed data because the processors are closer to the memory. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Consider **claim 7**, and as applied to **claim 6** above, Stacovsky in view of NPL1, NPL2, and Radke disclose the integrated circuit wherein the first type of access request is a memory write request *(Stacovsky: column 9, lines 3-5)*.

Consider **claim 8**, and as applied to **claim 7** above, Stacovsky in view of NPL1, NPL2, and Radke disclose the integrated circuit wherein the integrated circuit includes a memory interface unit operatively connected with, and under the control of, the timeslot arbitrator *(FIG. 9A-B, FIG. 14)*, and wherein the memory interface is operatively connected to: the respective operative units via respective data buses *(FIG. 9A-B, FIG. 14)*.

Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention that the memory via a memory bus can be of greater width than the communications buses, because it a design choice of which a smaller bus size can be cheaper and easier to manufacture because of less bus lines. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Consider **claim 9**, and as applied to **claim 6** above, Stacovsky in view of NPL1, NPL2, and Radke disclose the integrated circuit wherein the number of timeslots between the timeslot indicated by the lookahead pointer and the timeslot indicated by the current pointer takes into account a latency difference

between performing an access request of the first type and at least one of access request types *(Stacovsky: the timeslots or entries "take into account" the latency difference because they arrive in order of receipt even though relative to time one of higher latency could have been sent before a lower latency time request but received by the arbiter afterwards; NPL2: Furthermore, takes into account priority and latency: page 1)*.

10. **Claim 17** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")** in view of **Non-Patent Literature ("Southbridge – a whatis definition," Jason Rush, hereinafter "NPL1")** as applied to **claim 10** above, and further in view of **Radke et al. (US Patent # 6741253 B2, hereinafter "Radke")**.

Consider **claim 17**, and as applied to **claim 10** above, Stacovsky in view of NPL1 discloses the method wherein the requesters are hardware units and the method is implemented by a timeslot arbitrator *(FIG. 9A-B, 14)*.

However, Stacovsky may not specifically disclose wherein the requesters and time slot arbitrator are on an integrated circuit.

Radke discloses placing processors, memory, and memory controllers on an embedded/integrated circuit *(column 1, lines 14-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made integrate the entire processors, memory

and arbitrator in the system of Stacovsky in view of NPL1, because it is a design choice which increases throughput of processed data because the processors are closer to the memory. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

11. **Claim 18** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")** in view of **Non-Patent Literature ("Southbridge – a whatis definition," Jason Rush, hereinafter "NPL1")** as applied to **claim 10** above, and further in view of **Non-Patent Literature ("RIOT-The Scheduling Problem," hereinafter "NPL2")**.

Consider **claim 18**, as applied to **claim 10** above, Stacovsky in view of NPL1 discloses the method wherein each request can be one of at least two types, a first of the types having a higher latency associated with its performance than at least some of the other types *(it can but not necessarily does; in a system with different processors and memories it is inherit that that there will be access requests of varying latencies, such as different distances between specific processors and memories, and fabrication/manufacturing defects)*, the method including the steps of:

(c) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future

timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue; use of FIFO memory: column 18, line 19-20)*; and

(d) in the event an access request as arbitrated via the lookahead pointer, initiating performance of the access request earlier than the position in the list suggests it would be performed should it be started when the current pointer reached the timeslot *(command 3 is executed before command 2, but after 1: FIG. 14)*.

Stacovsky discloses the use of a FIFO and executing requests out-of-order if prioritized as discussed above, and asserts it is inherit to a FIFO to (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list. However, if the applicant references FIFO that does not maintains these pointers, Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention a First-in-first-out or ordered buffer allows (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue)*, because a use of these buffers are a well-known way of indicating order of requests to indicate priority based on order in which the entries were received. Furthermore, it would

have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Stacovsky orders based on timeslot and prioritizes certain requests, however, Stacovsky may not specifically disclose prioritizing based on if the request **is of the first type** (if first type, initiate performance earlier than normal position of FIFO).

Furthermore, NPL2 discloses a system which prioritizing higher latency requests earlier than normal ordered operation *(Longest Processing Time (LPT): page 1)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to prioritizing based on if the request is of the first type in the system of Stacovsky and NPL1, because NPL2 teaches the LPT is a heuristic used for finding the minimum makespan of a schedule and no one large job will "stick out" at the end of the schedule and dramatically lengthen the completion time of the last job *(page 1)*. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp *(LPT scheduling algorithm)*.

Response to Arguments

12. Applicant's arguments filed 01/07/2008 have been fully considered but they are not persuasive. See above rejections and further explanation below.

13. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection, necessitated by amendments to the independent claims.

Regarding Claim Objections

14. Prior claim objections have been removed due to applicant's amendments. It is noted however the amendments have introduced new claim objections. See above claim objections.

Regarding 35 USC 112, second paragraph Rejection

15. Prior claim rejections have been removed due to applicant's amendments. It is noted however the amendments have introduced new claim rejections under 35 USC 112. See above claim rejections.

Regarding 35 USC 102(e) and 103(a) Rejections

16. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection, necessitated by amendments to the independent claims.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW R. CHRZANOWSKI whose telephone number is (571)270-1176. The examiner can normally be reached on M-Th 7:30am-5:00pm, Every other Friday 7:30am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Matthew R Chrzanowski
Examiner
Art Unit 2186

/M. R. C./
Examiner, Art Unit 2186
4/9/2008